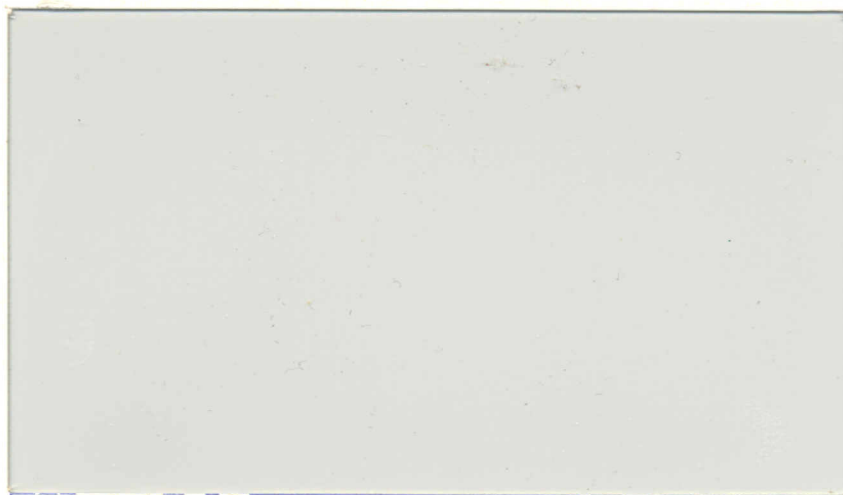




Product Number: 1000-01
Revision Number: 1.0
Date: 10/1/82

Section	Page
1. Introduction	1
2. Hardware Stack	2
3. Non-Volatile RAM	3
4. User Manual	4

QBX-FOG/C

HARDWARE STACK AND NON-VOLATILE RAM

USER MANUAL

All rights in this publication are reserved. No part of it may be reproduced or transmitted in any form without prior written permission. Except where noted, copyright vests with Quantum Electronics.

The information in this document is subject to change without notice. While every effort is made to ensure that the information contained in this document is accurate, Quantum Electronics does not assume any responsibility for any errors that may occur.

Quantum Electronics (QEC) has assumed no responsibility for the use of any circuitry other than the circuitry specified in a product manual issued by QEC or its subsidiaries (QEC) Ltd.

QEC and its subsidiaries (QEC) Ltd. make no warranty on the fitness of this product for specific purposes.

QEC, QEC Ltd, QEC International, and QEC Ltd are trademarks of QEC Ltd.

All products are warranted against defects in materials and workmanship under normal use and in their original condition. If found defective by QEC Ltd, the warranty period is 90 days from the date of purchase. The warranty period is 90 days from the date of purchase. The warranty period is 90 days from the date of purchase.

(c) Copyright October 1982 Quantum Electronics
QEC Ltd, Box 1000,
Johannesburg, South Africa
Tel: 011-435-1000

QBX-FOG/C

Product:- QBX-FOG/C
Product Number:- 1003
Manual Number:- 1003-01

Chapter	Rev	Note
All	1.0	1

Notes:-
1.Original Document

All rights to this publication are reserved. No part of it may be copied or reproduced in any form without prior written consent. Except where noted copyright vests with Quantum Electronics.

The information in this document is subject to change without notice. Whilst every effort is made to ensure that the information contained in this document is correct, R & D Electronics (Pty) Ltd assumes no responsibility for any errors that may occur.

R & D Electronics (Pty) Ltd assumes no responsibility for the use of any circuitry other than the circuitry embodied in a product manufactured by R & D Electronics (Pty) Ltd.

R & D Electronics (Pty) Ltd makes no warranty on the fitness of this product for a specific purpose.

iSBX, iSBC, Multibus, MULTIMODULE, and Intel are trademarks of Intel Corporation.
Z80 is a trademark of Zilog Inc.

All products are warranted against defects in material and workmanship under normal and proper use and in their original and unmodified condition. If found defective by R & D Electronics (Pty) Ltd within the terms of this warranty, the sole obligation of R & D Electronics (Pty) Ltd shall be to repair or replace (at the option of R & D Electronics (Pty) Ltd) the defective product. The warranty period is 90 days from delivery of the product.

(c) Copyright October 1982 Quantum Electronics,
c/o R & D Electronics (Pty) Ltd
P.O. Box 61903,
Marshalltown 2107,
Johannesburg, South Africa.
Telex: 8-3046 Phone: 8341204

Rev:1.0

CONTENTS

	PAGE		PAGE
CHAPTER 1		CHAPTER 2	
GENERAL		PRINCIPLE OF OPERATION	
Introduction	1.1	Introduction	2.1
Description	1.1	QBX Bus Interface	2.1
Equipment supplied	1.1	Circuit Description	2.1
Specifications	1.2	Stack Counter	2.1
		Memory Access	2.2
		Push	2.2
		Pop	2.2
		Wait State Generation ...	2.2
		MRESET, Power Fail, and	
		Battery Recharghe	2.2
 CHAPTER 3		 CHAPTER 4	
PROGRAMMING INFORMATION		PREPARATION FOR USE	
Introduction	3.1	Introduction	4.1
Stack Counter	3.1	Unpacking	4.1
Push	3.1	Mounting	4.1
Pop	3.1	Battery	4.1
Summary of Functions	3.2		
Applications	3.2		
 CHAPTER 5			
SERVICE INFORMATION			
Introduction	5.1		
Parts List	5.1		
Schematics	5.2		
 APPENDIX			
Appendix A			
Expanding the Storage Capabilty.....		A.1	

TABLES		
Table	Title	Page
3.1	Summary of Functions and their Associated Addresses	3.2

CHAPTER 1 GENERAL

Introduction

The QBX-FOG/C board is one of a growing range of iSBX bus compatible boards manufactured by Quantum Electronics. These boards are designed to increase the number of functions in a Multibus system without having to resort to the addition of a full sized Multibus card to achieve that function. This document provides all the information required to use the QBX-FOG/C.

Description

The QBX-FOG/C is a method of introducing a non-volatile storage facility on a Mutlibus card. It is configured as a 256 byte hardware stack. This configuration as a stack provides extra capabilities and simplified programming for the software designer. Any address within the memory range may be programmed as the starting address allowing random access to any location in storage.

The contents of the stack are retained by an off board battery (not supplied) powering a CMOS RAM (Complimentary Metal Oxide Semiconductor Random Access Memory).

Equipment Supplied

The QBX-FOG/C is shipped in a padded package. Included in this package are a plastic spacer and two plastic screws to mount the QBX board on to the host SBC computer.

Specifications

Access Time:

Read stack address 40nS

Write stack address 50nS

Read and write data 400-500nS

Addressing Range:

The QBX-FOG/C is compatible with any board that supports the Intel iSBX bus. The addressing range of the QBX-FOG/C is derived from this host board.

Interface:

System Bus Compatible with the SBX bus specifications. See Intel publication 142686-001

Battery Backup Screw terminal.

Power Requirements:

5 Volt +/-5% @502mA (worst case).

Standby current drain 2.1mA (worst case).

Environment:

Operating temperature 0-55 degrees Celsius, humidity to 90% non-condensing.

Size:

Width 724 mm (2.85 in)

Length 943 mm (3.71 in)

Height 20 mm (0.79 in) including QBX connector

Weight

CHAPTER 2 PRINCIPLE OF OPERATION

Introduction

This chapter describes the operation of the QBX-FOG/C. The SBX bus is essentially an I/O bus and as a result one cannot access 256 bytes in a straightforward manner as there are only a maximum of 4 lines and not the required 8. To solve this problem the QBX-FOG/E is configured as a stack. Each address can be individually addressed allowing random access to any part of the stack. Whilst the original intention was to provide a method accessing memory, there is a considerable advantage from a software viewpoint in having an additional stack in the system.

Whilst the QBX-FOG/C was designed to provide 256 bytes of nonvolatile storage, the device used is a 2K x 8 CMOS RAM. Appendix A details how the full capacity of the RAM may be used.

QBX Bus Interface

Detailed description of the iSBX bus is contained in the Intel publication 142686-001. Users are referred to this document for a clearer understanding of the signals used. The QBX-FOG/C uses the following signals: MD0-MD7, IORD/, IOWR/, CS0/, CS1/, MRESET, MCLK, MWAIT, and of course 5v, ground and MPST/.

Circuit Description

In essence all the QBX-FOG/C consists of is an 8 bit programmable up/down counter driving a CMOS RAM.

Stack Counter:

The stack counter is made up of two 74LS193 programmable up/down counters. The 2 x 4bits drive the address inputs of a 2Kbyte CMOS RAM. Taking CS1/ active simultaneously with the IOWR/ signal generates a signal LOAD AD/ (IC10/11) which strobes the contents of the data bus onto the counters. D7 corresponds to the most significant address bit.

When CS1/ and IORD/ are active the signal READ AD/ goes active and enables the output of the 2 counters (and hence the stack counter value) on to the data bus via the octal buffer IC3.

Reading this the stack counter does not affect its value and can be done at any time.

Note:

The outputs of the counters do not address the RAM in a logical sequence; for instance the least significant bit of the counters IC1/3 goes to pin 2 of the RAM. Pin 2 according to the RAM data sheet is in fact A6, but this in fact will make no difference to the operation of the circuit. This change in convention is transparent to the user and was done for the convenience of designing the printed circuit board.

Memory access:

Whenever CS0/ and either read or write commands are active, the on board memory is accessed.

Push:

Writing to the memory is akin to a "push" operation in a normal stack. The information on the data bus is stored at the location addressed by the stack counter. The trailing edge of the IOWR/ signal is delayed by the RC network R14,C3 (to meet address hold requirements) and clocks the count up (IC1/4) line of the counters. The memory will store the next byte at this new address unless the counter is reprogrammed or is "popped".

Pop:

Reading from the RAM is akin to "popping". When CS0/ and IORD/ are simultaneously active MRD/ (IC9/8) goes active, enabling the OE input of the RAM. A similar signal (IC10/6) clocks the monostable IC5/3 on its leading edge. The trailing edge of the Q/ output (IC5/1) clocks the count down input of the stack counters (IC1/5). The counters are decremented by 1 and it is the value at this new address that is read by the microprocessor.

Reading from location 00 will loop back and return the value of location FF hex. Writing to location FF will store to that location and increment the counter to 00. To allow for the propagation delays on reading, several wait states are introduced.

Wait state generation:

The 10 MHz MCLK signal is applied at the clock input (IC11/8) of a serial to parallel shift register. The serial in lines are held high. When CS0/ goes active it enables the shift register and a NAND gate (IC10/2). The other input to this gate is derived from the output of the shift register. Each successive output of the shift register has a "1" shifted on to it every 100 nS. The time delay until MWAIT/ (IC10/3) goes inactive may be user programmed, but is shipped set to 400-500nS.

MRESET, Power Fail, and Battery Recharge

When MRESET is active or when the supply voltage through the QBX connector drops below a certain value the signal EN (IC4/1,2) goes inactive. This inhibits the chip select and write signals to the RAM.

The RAM requires a minimum of 2.7 volts supply voltage at the screw connector (less if diode D1 is replaced by a Germanium device). The voltage Vcc is compared to the battery voltage through an LM339 comparator. Whilst Vcc is greater than a pre-programmed amount transistor Q1 is turned on, providing Vcc to the supply pin of the RAM. When changeover occurs the RAM takes its supply from the standby battery through diode D1. The standby battery is charged from Vcc through diode D2 and resistor R11. The QBX-FOG/C is shipped with R11 set at 82 ohms.

The values of R10 and R11 are chosen for a 3.6 Volt battery, to allow detection of a power fail when the supply voltage drops below 4.5 volt. Should other battery voltages be used, the value of the resistors should be adjusted according to the following

formula:

$$\frac{V_{batt} * R_6}{R_6 + R_5} = \frac{4.5 * R_8}{R_7 + R_8}$$

Bear in mind that whilst charging the voltage of the battery may marginally increase.

If it is required that the battery be charged from a separate source or that it be non-rechargeable either or both R8 or D2 may be removed.

CHAPTER 3 PROGRAMMING INFORMATION

Introduction

This chapter describes the programming and possible applications of the QBX-FOG/C.

Stack Counter

Setting up the Stack Counter is merely a case of writing the wanted address on the stack to any address in the range X8-XF hex, where X depends on the host board. For example, to programme address 57 hex on the stack addresss where the host board space for the QBX module is C0 to CF hex, an assembly programme would appear similar to the following:

```
MVI A,57H
OUT 0C8H
```

To read the stack counter is simply a read instruction such as:

```
IN 0C8H
```

and the accumulator will contain the contents of the stack counter.

Push

In order to save information in the RAM a push sequence must be executed. The byte that is required to be stored is written to any location from X0 to X7 hex, X is set by the host board. This byte is stored at the address currently on the counters. At the termination of this instruction the counters will have been incremented by 1. To store 98 hex on the stack with the same conditions above example:

```
MVI A,98H      ;stack counter at 34 hex say,
OUT 0C0H       ; stack counter now at 35 hex
```

Pushing at location FF rolls around to loaction 00.

Pop

To extract information from the RAM a read from location X0 to X7 hex is executed. The current address pointer is decremnted and the information from this new location is fed to the accumulator.

```
IN 0C0H        ;stack counter at 35 hex
               ;stack counter at 34 hex and
               ;if from above example accumulator=98
```

Popping from location 00 reads back from location FF hex.

Summary of Functions and Addresses

Table 3.1 provides a summary of the functions and their associated addresses on the QBX-FOG/C.

HEX	Add.	Read	Write	Counter	Action
X8 - XF			@	Data -> Counter	Load stack counter
X8 - XF	@			Counter -> Data	Read stack counter
X0 - X7			@	N -> N+1	Write byte to loc- N. "PUSH".
X0 - X7	@			N -> N-1	Read byte at loc- ation N-1. "POP".

Note:

X is the most significant nibble of the hex address and is determined by the host board.

@=active

Table 3.1
Summary of the Functions and their Associated Addresses

Applications

A major advantage of a stack is that the programmer does not have to be aware of the location of a particular byte, just that it is there when he needs it. Since the stack counter is fully programmable sections of the RAM may be utilised for storage of data in power fail circumstances while the rest may be used for even multiple stacks.

Most microprocessors (and certainly the 8085 and Z80) allow only a single stack in their architecture. As a result passing parameters from routine to subroutine may be complicated, especially when some have to be reentrant. By using one or more extra stacks the problem is largely simplified.

Further information may be conveyed by using the capability of reading the stack counter. For example, if a routine required that a variable length message be sent to a VDU (visual display unit). The parameters (the message) are pushed onto the stack in reverse order starting say, at location 00. As the transmitting device becomes ready for a new character, it is popped off the stack. when the stack counter reaches its original value, 00 the message is complete.



CHAPTER 4 PREPARATION FOR USE

Introduction

This chapter provides information on the installation of the QBX-FOG/C on a host SBC board.

Unpacking

The QBX-FOG/C is shipped in a padded packet together with 1 plastic spacer and 2 plastic screws.

On receipt of the package inspect immediately for signs of damage, water or any other signs of mishandling. If there are any of these signs contact your carrier or his agent, or the local Quantum Electronics representative. If you do open the package, please retain the packaging.

Mounting

The QBX-FOG/C will mount on any SBC computer that allows an iSBX board. Affix the spacer with one of the screws to the host board. Mount the spacer in the hole corresponding to the hole just to the side of R5 on the QBX board.

The QBX-FOG/C should now be mounted on the mating connector and affixed to the host board with the remaining screw.

When a QBX card is mounted on a host card, the resulting structure occupies an additional card slot above the SBC card. Bear this in mind when you allocate slots in a cardframe.

Battery

Prior to applying power connect a 3.6V NiCd battery to the screw terminals, positive to terminal 1 and ground to terminal 2. This assumes no modifications have been made to the circuitry as discussed in preceding chapters.

CHAPTER 5 SERVICE

Introduction

This chapter provides a parts list and schematic diagram of the QBX-FOG/C.

Parts List

Semiconductors:

IC1,2	prog. up/dwn counter	74LS193
IC3	octal buffer	74LS245
IC4	quad comparator	LM339
IC5	monostable multivibrator	74121
IC6	hex inverter	74S04
IC7	2Kx8 CMOS RAM	HM6116LP-3
IC8	Fairchild hex inverter	74LS04 or 74F04
IC9	quad NAND gate O.C.	74S03
IC10	quad NAND gate	74S00
IC11	serial to pll s.r.	74LS164

Q1	PNP transistor	2N2905A
----	----------------	---------

D1,2	general purpose diode	1N4001
Z1	400mW zener diode	5V6

Capacitors:

C1,2,4,6,7	ceramic	0.01uF
C3	ceramic	330pF

Resistors:

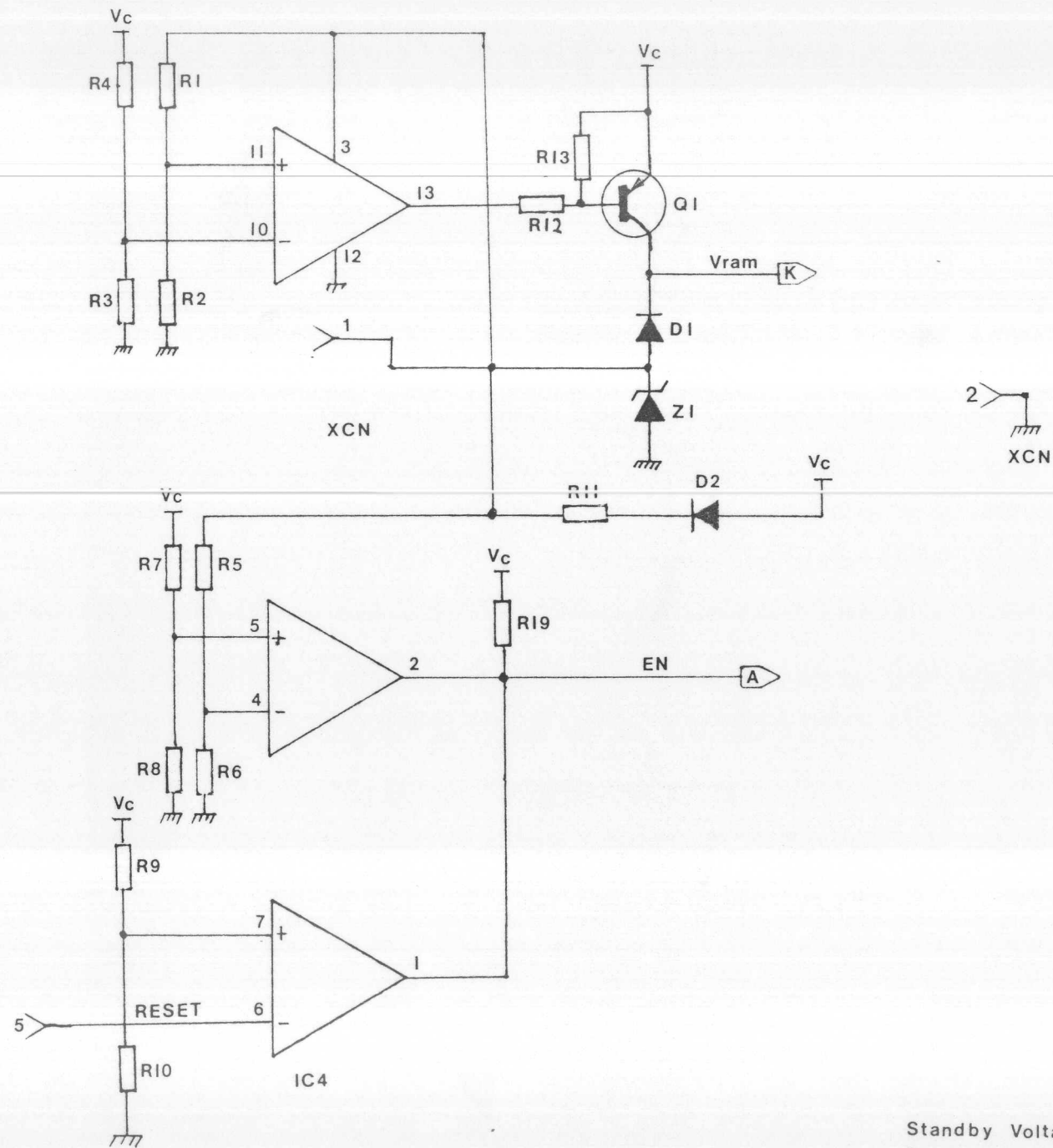
R1-4	1/4W 2%	200Kohm
R5	1/4W 2%	120Kohm
R6,10	1/4W 2%	100Kohm
R7	1/4W 2%	68Kohm
R8	1/4W 2%	47Kohm
R9	1/4W 2%	180Kohm
R11	1/4W 2%	82 ohm
R12	1/4W 2%	820 ohm
R14	1/4W 2%	10 ohm
R15-18	1/4W 5%	1Kohm
R19	1/4W 2%	22Kohm

Connector:

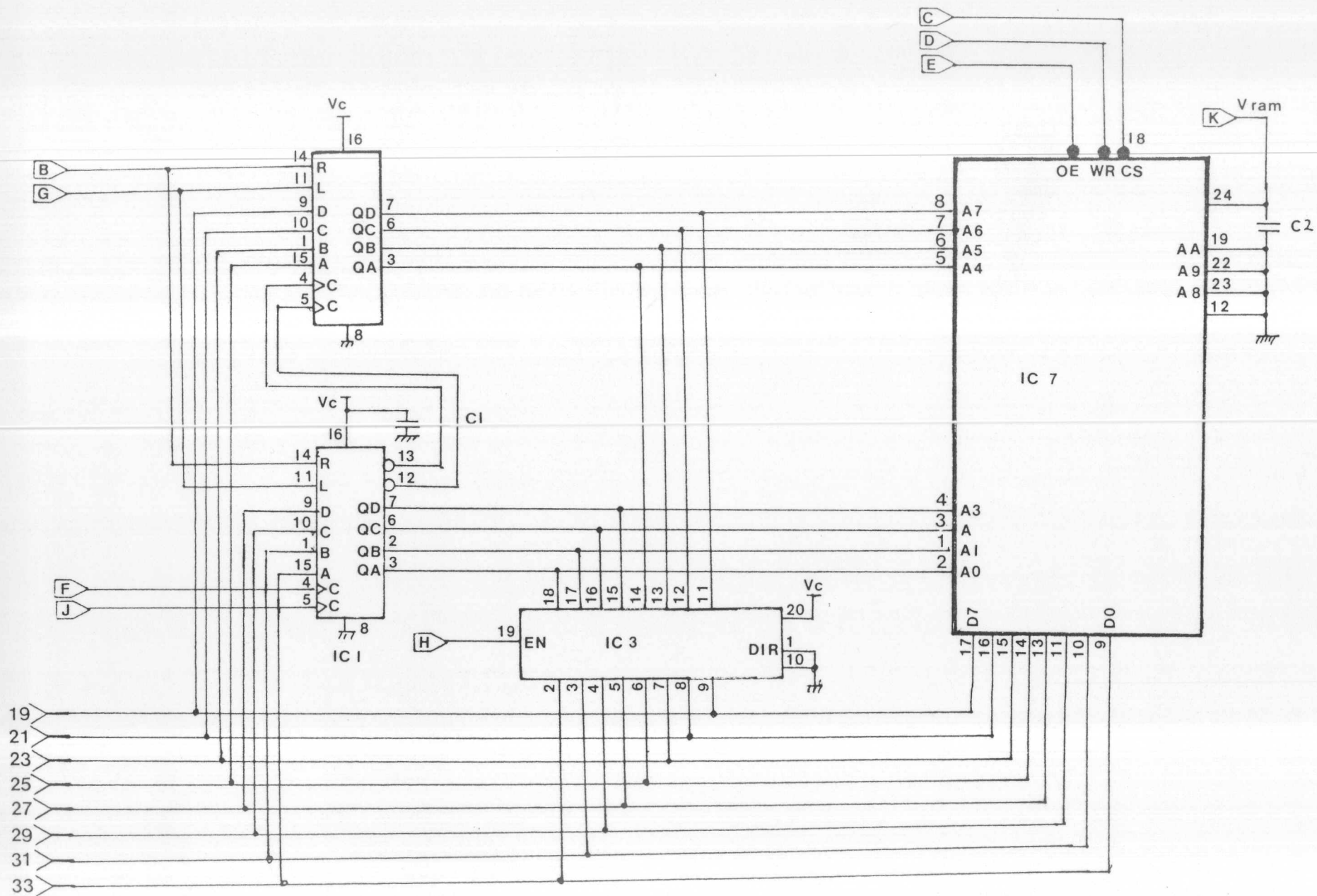
36 way SBX Viking	LMP01KH18A01
2 way screw RIA	Typ 0101 5mm

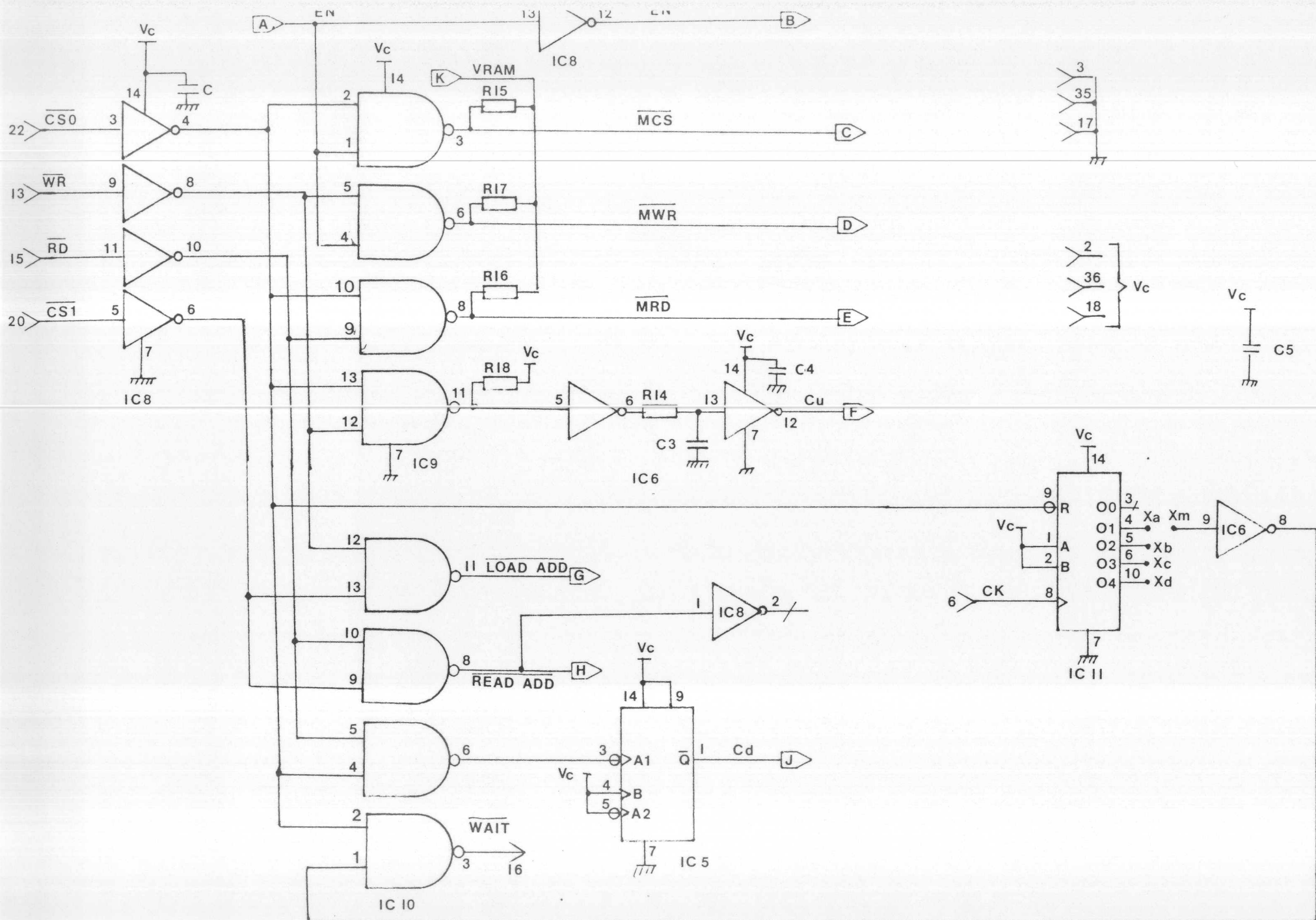
Unused parts:

R13
C5



Standby Voltage and
Power Failure Detection
Sheet 1 of 3
1003-02
Rev: 1.0





APPENDIX A
EXPANDING THE STORAGE CAPABILITY

It has been suggested that to utilise the full 2K x 8 capability of the RAM certain modifications to the circuit be made. This would then enable the stack to be configured as 8 banks of 256 bytes. This could of course lead to complications in bank selection vis-a-vis current stack pointer.

The modification is simply breaking the tracks that hold A8, A9 and A10 to ground (pins 23, 22, and 19) and connecting these to MA0, MA1 and MA2 on the QBX connector (pins 11, 9, and 7).

If you would just like to experiment before cutting the traces, you could just lift the relevant pins from their socket.

If you would like to see this as a permanent feature of the QBX-FOG/C please fill in the relevant part on the questionnaire at the back of this manual. (We hope you will fill this form in anyway!)

